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1. A PHASE LOCKED LOOP LOCK CONDITION DETECTOR
TRODDEN, Thomas / KONINKLIJKE PHILIPS ELECTRONICS N.V., *PATENT COOPERATION TREATY APPLICATION*, Jul 1999
...output 113 of **XOR gate** 115 and shift...signals. When the **PLL** is in lock, as...output 113 will be **logic** high. Consequently...section 180 will be **logic** high. If the **PLL** becomes out of...output 113 of **XOR gate** 115 will switch to **logic** low for one or...
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2. DIGITAL PHASE LOCK LOOP AND SYSTEM FOR DIGITAL CLOCK RECOVERY
RUNALDUE, Thomas, J. / ADVANCED MICRO DEVICES INC., *EUROPEAN PATENT*, Dec 1998
...and the output **logic** 36 then changes...transitions from a high **logic** level to a low **logic** level, to transition...acquisition, the digital **PLL** proceeds with the...the edge detection **comparator** 26 replaces the...flip-flops and an **XOR gate** (not shown) for...
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3. SINGLE-ENDED PULSE GATING CIRCUIT
LLEWELLYN, William, D. / NATIONAL SEMICONDUCTOR CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Sep 1994
...108, a low pass **filter** (LPF) 109, and...VCO) 110. Phase **comparator** 108 compares...respectively. Phase **comparator** 108 then generates...after being **filtered** by LPF 109, causes...line 105. If **PLL** 100 is properly...represents a **logic** one while the...referred to as data **latch** 101), is provided...
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4. Les effets de l'expérience collectiviste sur l'identité, le comportement politique et l'éthique du travail des paysans ...
Vultur, Mircea., Jan 1970
...PERFORMANCE CONTINUOUS-TIME **FILTERS** FOR INFORMATION TRANSFER SYSTEMS...Performance Continuous-time **Filters** for Information Transfer Systems...197 6.4.2 **Comparator**...2 A host of applications of **filters**...
Full text thesis available via NDLTD
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5. HIGH PERFORMANCE INTER - CHIP [PDF-248K]
Oct 2001

Did you me
logic compa
"match filte

Your query
logic AND c
"xor gate" A
filter AND p
We did this
quotes to c
and by rem
essential w
- Repeat v

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using thes
found in t
controlled c
control volt
data input
flip-flop
floating gat
frequency s
impedance
incoming si
output sign
phase comp
phase error
power dissi
programma
reference v
rising edge
transmitter

Or refine
All of the

...68 4.3.4 Amplifier and **Latch** Design...5: Integrate-and-dump **filter** phase characteristics...and integrate-and-dump **filter**...Figure 4.16: Amplifier and **latch** schematic...supply step response of a **PLL** and DLL...
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Jun 1998
The Programmable **Logic** Data Book April 1998 , XILINX, XACT, XC2064...NeoCAD EPIC, NeoCAD PRISM, NeoROUTE, Plus **Logic**, Plustran, P+, Timing Wizard, and TRACE...Foundation Series, BITA, Configurable **Logic** Cell, CLC, Dual Block, FastCLK, FastCONNECT...
[http://jason.sdsu.edu/xilinx/wcd029b6.pdf]
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...68 4.3.4 Amplifier and **Latch** Design...5: Integrate-and-dump **filter** phase characteristics...and integrate-and-dump **filter**...Figure 4.16: Amplifier and **latch** schematic...supply step response of a **PLL** and DLL...
[http://www-vlsi.stanford.edu/papers/ss_thesis.pdf]
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☐ **9.** MULTIPLE CHANNEL ADAPTIVE DATA RECOVERY SYSTEM
TALAGA, Ronald, F., Jr. / VITESSE SEMICONDUCTOR CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Sep 2001
...the data channel **latch** 47a is generated...monitor channel **comparator** 41b for comparing...monitor channel **comparator** 41b is provided to a monitor channel **latch** 47b. The monitor...transitions from a **logic** 0 state to **logic**...the output of the **XOR gate** is a **logic** 1 when...
Full text available at patent office. For more in-depth searching go to LexisNexis
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☐ **10.** Xilinx 1998 Data Book (4/98) [PDF-3MB]
Apr 1998
The Programmable **Logic** Data Book April 1998 The Programmable **Logic** Data Book 2100 **Logic** Drive San Jose, California 95124 United States of America Telephone: (408) 559-7778 Fax: (408) 559-7114 R Xilinx Home Page (WWW): http://www.xilinx.com/ ("Answers...
[http://www.it.lth.se/courses/dsi/material/Labs/DATABOO...]
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☐ **11.** DIGITAL PHASE LOCK LOOP AND SYSTEM FOR DIGITAL CLOCK RECOVERY
RUNALDUE, Thomas, J. / ADVANCED MICRO DEVICES, INC., *PATENT COOPERATION TREATY APPLICATION*, Sep 1997
...and the output **logic** 36 then changes...transitions from a high **logic** level to a low **logic** level, to transition...acquisition, the digital **PLL** proceeds with the...the edge detection **comparator** 26 replaces the...flip- flops and an **XOR gate** (not shown) for...
Full text available at patent office. For more in-depth searching go to LexisNexis
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☐ **12.** DARPA Spring 1993 Semiannual [87K]
John F. McDonald, Feb 1997
...efficiently use a small set of **logic** units. Industrial assessments...as well as the underlying **logic** circuit class, namely full...feedback shift registers (LFSRs), **comparators**, and multiplexers, besides the control **logic** for selection of a test and...
more hits from [http://www.ecse.rpi.edu/research/mcdonald/frisc/report...]

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☐ **13.** Electronic data storage and retrieval apparatus and method
Davis, Charles Lawrence / ABBOTT LABORATORIES, *EUROPEAN PATENT*, Jul 1987
...input/output gating **logic** circuits of the data...of the servo control **logic** of the data link device...schematic diagram of the **PLL** counter and decode **logic** circuits shown in FIG...diagram of the magnitude **comparator** and RF gain counter...
Full text available at patent office. For more in-depth searching go to LexisNexis
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☐ **14.** CLOCK SIGNAL DISTRIBUTION SYSTEM
MILLER, Charles, A. / BEDELL, Daniel, J. / CREDENCE SYSTEMS CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Jul 1997
...16(2)- 16(N) **latch** the data pulse...consisting of a phase **comparator** 24 and a loop **filter** 26. The incoming...Loop **filter** 26 **filters** (integrates) the phase **comparator** 24 output signal...**comparator** 24. Phase **comparator** 24 and loop **filter** 26 operate together...
Full text available at patent office. For more in-depth searching go to LexisNexis
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☐ **15.** DIGITAL PLL SYSTEM AND FAST FREQUENCY SWITCHING METHOD
ZUTA, Marc / ZUTA, Idan / ZUTA, Marc, *PATENT COOPERATION TREATY APPLICATION*, Nov 2000
...magazine, pp. 94-108, titled "A New **PLL** with Fast Settling Time and Low...found that a phase-lock loop **PLL** using a fast phase difference...difference. Usually the low pass **filter** LPF in the loop is set to a slower...practical applications, however, the **PLL** is required to respond faster...
Full text available at patent office. For more in-depth searching go to LexisNexis
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☐ **16.** No Title [PDF-463K]
Jul 1996
...input-to-output ratio for best **logic** effi- ciency. The GLB (figure...of Both Wide and Narrow **Logic** Functions High-Speed Bypass...Architecture u Great for Counters, **Comparators** and ALU Func- tions Single PT Configuration u Small **Logic** Functions at Fast Speed...
[http://digital5.ece.tntech.edu/public/611/Clements%20C...]
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☐ **17.** front1.pdf [PDF-634K]
Jun 2001
...49 4.4.1.2 The use of **Filters** to avoid noise aliasing in the system...5.1.2 Impedance Matching to External **Filters**...76 5.4 The ADC Buffering and **Filtering** Stage...
[http://bwrc.eecs.berkeley.edu/Publications/1995/theses...]
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☐ **18.** No Title [PDF-859K]
Jul 1996
...density programmable **logic**. Lattice's ispLSI...high-density programmable **logic** standard of the 1990's...Phase Locked Loops (**PLL**) in High Speed Designs...to Generic Array **Logic**...9-5 **Latch**-Up Protection...Fundamentals of Digital **Filter** Design...
[http://www.ece.tntech.edu/Public/611/Clements%20CDROM/...]
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☐ **19.** Newsgroups: news.answers,comp.answers,comp.robotics [ASCII-147K]
Dec 1995
Path: senator-bedfellow.mit.edu!bloom-beacon.mit.edu!hookup!news.mathworks.com! newsxfer.itd.umich.edu!chi-news.cic.net!usc!math.ohio-state.edu!cis.ohio-state.edu! nntp.sei.cmu.edu!bb3.andrew.cmu.edu!cantaloupe.srv.cs.cmu.edu!nivek From: nivek@cs.cmu.edu (Kevin Dowling) Newsgroups: news.answers,comp.
[http://ftp.uni-stuttgart.de/pub/doc/faq/comp/robotics/...]
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☐ **20.** titl_fly.p65 [PDF-628K]
Aug 2000

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